**Actual development using Xilinx FPGA XCVU37P**

**Tipalo has created a completely digital bio-mimetic model of the brain,**
by taking the biological neural nets as a template for software development,
enabling hereby living machines, which can act fully autonomous,
being capable of self-learning, only by reacting with the environment.

**"Many small things, which react permanently with each other in a space, build together a big object."**
This is the basic underlying principle of our digital biomimetic model of the digital brain:
Therefore, our model creates an own space and time flow, where objects can interact with each other,
while the self-learning mechanism is the result of the internal interaction between the neural nets.

**Time based pattern logic, programmed in VHDL for FPGA SiPs as neural nets,**
This biological inspired technology is digitally implemented in hard- and software,
which form together higher forms of organizational structures and hierarchies,
used as ANS - Artificial Nervous Systems, with own self-learning mechanism.

**We are currently developing a VHDL based operating system for real-time applications, in an FPGA**.
This operating system is simulating the basic functionality of a biological brain, can build together neural nets and higher forms of organization. So, only one type of neural nets can be performed, namely Tipalo own **SPNNs, Self-Programmable Neural Nets, connected via SPNoC, Self-Programmable Network on Chip.**

**Within this VHDL operating system, all neural nets build together an ANS, Artificial Nervous System,**
similar to the biological nervous system of any living multicellular organism on Earth. This ANS enables SLM, Self-Learning Mechanism, which accumulates knowledge, while this can be stored and retrieved on demand.
**Knowledge does not change very often, therefore NVRAM can and will be used for this purpose.**

**We are using a FPGA SiP, System in Package, consisting of a high capacity FPGA and 2 HBM2 dies,**
each with a capacity 4 GBytes of RAM. In addition we also support external DDR4 memory interfaces.
The use of FPGA is required due to the massive parallel programming, in order to process neural nets, means no CPUs or MCUs are used within the FPGA, only hard IP, e.g. multi-Gigabit Ethernet interfaces.

**Each HBM2 has a memory bandwidth of 230 GBytes, implying 460 GBps in total for the entire SiP.**
This is necessary in order to process thousands of individual neural nets in parallel and simultaneously, whle using all of the distributed and on-chip Block RAM, while processing all active neurons merely within 1 ms.
The brain capacity and processing speed is only limited by the SiPs memory capacity and bandwidth.

**We need additional NVRAM, to store externally the ANS, as well as the FPGA configuration bitstream,**
with actually 8 GB HBM2 and 256 GB external DDR4 memory, while the working frequency is only 125 MHz.
The power required is between 50 and 200 Watts, while the footprint of the FPGA SiP is 55 x 55 mm, which reduces the corresponding usage to applications located in data centers, not suitable for embedded systems.

**Required system with 3DSoC**

**Having ReRAM, external storage is no longer required, thus eliminating HBM2 and DDR4 memory,**
enabling herewith the usage of only 3DSoC technology, without the need of any further memory or logic ICs.
Via the same Ethernet interfaces, we can connect several brains, each having very low power consumption, as only max.10% of the total brain capacity is used, by processing merely the simultaneously active neurons.